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2D Steep-Slope Tunnel Field-Effect Transistors Tuned by van der Waals Ferroelectrics

Xinrui Chen, Tiantian Jiang, Hanbin Wang, Yang Wang, Miao Zhang, Yi Cui, Yong Wang, Nannan Li, Xinchuan Du, Chaoyi Yan, Yuqing Liu,* and Xianfu Wang**

sPower consumption has emerged as a central concern in the realm of complementary metal-oxide-semiconductor (CMOS) technology. Silicon-based semiconductor devices have now approached the fundamental thermionic limit of the subthreshold swing (SS), which is 60 mV dec^{-1}, as defined by the Boltzmann tyranny. Tunnel field-effect transistors (TFETs) are considered promising low-power devices due to the band-to-band tunneling mechanism, which effectively avoids the thermionic limit. However, TFETs require the establishment of a staggered band alignment and currently lack effective techniques for adjusting the band offset. Here, by harnessing the robust ferroelectric field inherent to 2D $CuInP_2S_6$ (CIPS), a 2D WSe_2/MoS_2 heterojunction as well as a WSe_2 homojunction TFET controlled by ferroelectric gate are presented. The newly developed TFET achieves an ultra-low SS of 14.2 mV dec^{-1} at room temperature, an on/off current ratio exceeding 10^8, and a minimal hysteresis window below 10 mV. Additionally, the device demonstrates gate tunable negative differential resistance (NDR) characteristics with a very large peak-to-valley current ratio (PVCR) of 10.56 at room temperature. These findings underscore the significant promise of 2D ferroelectric tuning heterojunction and homojunction for future low-power electronic applications.

1. Introduction

Power consumption poses a significant barrier to the advancement of future CMOS chips, as it directly impacts processing speed and heat dissipation efficiency.[1–7] However, the subthreshold swing (SS), a critical indicator of power consumption in conventional MOSFETs, is limited to a value of 60 mV dec^{-1} at room temperature due to the inherent thermal characteristics associated with carrier injection.[8,9] Presently, there are various types of devices, such as tunnel field-effect transistors (TFETs), negative capacitance field-effect transistors (NCFETs), cold source field-effect transistors (CS-FET), and impact ionization field-effect transistors (IFET), which have demonstrated the ability to overcome the restriction imposed by thermal emission.[10–13] From the perspective of advancing carrier transport strategies, TFETs, featuring staggered band alignment between the source and channel to promote carrier mobility through the tunneling effect, demonstrate potential in overcoming this limitation.[14,15] However, prior to its feasible integration into practical applications, several hurdles should be navigated.[10] First, the inadequate modulation of the electrostatic gate impedes the formation of favorable band alignment conducive to tunneling. Furthermore, dangling bonds in bulk materials frequently result in interfacial defects and lattice mismatches, which also detrimentally impact the SS. Therefore, the selection of appropriate materials for TFET construction that can achieve a staggered bandgap alignment and simultaneously enable optimal device performance free from interface issues has indeed become a critical concern.

The advancement of 2D materials presents significant opportunities for TFETs due to their atomic-thin characteristic, allowing for a potent electrostatic control.[16–22] Additionally, 2D materials exhibit unique ability to facilitate the arbitrary stacking of various functional materials without requiring lattice matching, attributable to the weak interactions known as van der Waals forces.[23–28] Coupled with an appreciably larger surface-to-volume ratio, these TFETs incorporating 2D materials offer the advantage of enhanced electrostatic control from the gate,

X. Chen, T. Jiang, Y. Wang, M. Zhang, Y. Cui, Y. Wang, X. Du, C. Yan, Y. Liu, X. Wang
State Key Laboratory of Electronic Thin Film and Integrated Devices
University of Electronic Science and Technology of China
Chengdu 610054, P. R. China
E-mail: yangwang@uestc.edu.cn; yuqing_liu@uestc.edu.cn; xfwang87@uestc.edu.cn
H. Wang, N. Li
Microsystem & Terahertz Research Center
China Academy of Engineering Physics (CAEP)
Chengdu 610200, P. R. China
H. Wang, N. Li
Institute of Electronic Engineering
China Academy of Engineering Physics (CAEP)
Mianyang 621900, P. R. China

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increased conductivity, and excellent interface contact with the gate insulator.[29] For example, previous researches have elucidated that the substitution of traditional silicon with atomic-thin MoS_2 in the channel presents the potential to fabricate vertical heterostructure MoS_2/Ge TFET with exceptional electrostatics and strain-free heterointerfaces, achieving an average SS of 31.1 mV dec^{-1}.[30] Subsequently, in an endeavor to ameliorate the issue of lower conduction current levels, researchers have developed TFETs based on black phosphorus (BP).[31] Due to the advantageous property of BP, where its thickness can spatially vary without yielding interface-related issues, this bulk BP/monolayer BP device exhibits a higher on-current with an average SS of 26 mV dec^{-1}. Despite some progress, the integration of few-layer 2D materials with bulk or 3D materials is inevitably affected by irregularities in the thickness and doping level of the semiconductor channel, significantly increasing the process complexity and hindering the full exploitation of the advantages of 2D materials. While in the case of 2D TFETs, it is essential to design the gate to achieve control over the band alignment. Firstly, conventional control gates are excluded from our consideration due to their reliance on deposition techniques, such as atomic layer deposition (ALD) which often unavoidably introduce interface defects.[32] In regard to 2D dielectric materials, represented by hexagonal boron nitride (h-BN), it has been demonstrated that they are capable of coupling with 2D channel materials, thereby providing a potential approach for the design of 2D TFETs.[33] Despite successfully addressing interface issues inherent in the manufacturing process, their modulation capacity falls short of realizing high-quality TFETs. In contrast, the novel van der Waals ferroelectric materials exhibit stable and strong polarization characteristics, suggesting the potential to construct control gates with robust modulation abilities while maintaining a clean interface.[34–37]

Our device design strategy incorporates $CuInP_2S_6$ (CIPS) as the controlling gate, with WSe_2 and MoS_2 serving as channel materials. The objective is to enhance gate control over the electrostatics of the tunnel junction while ensuring the clean interface. As one of the rare room-temperature 2D ferroelectric materials, CIPS exhibits switchable polarization at a thickness of approximately 4 nm and low leakage current. Its out-of-plane polarization has been extensively exploited in diverse nanoelectronic applications, effectively combining the robustness of ferroelectricity with the flexibility of van der Waals integration.[38,39] While for the channel materials, WSe_2 and MoS_2 were selected due to their well-established processing techniques. Furthermore, experiment evidence from both homojunction and heterojunction studies confirms their ability to manifest tunneling phenomena under gate modulation.[22,40–42] Consequently, they are considered suitable candidates for TFETs. Expanding on this groundwork, there is still a lack of compelling evidence and exploration concerning the integration of 2D ferroelectric gate with 2D semiconductor channels to create robust TFETs. This is precisely the focal point of our work that we endeavor to elucidate.

This article presents the successful fabrication of 2D van der Waals TFETs based on WSe_2/MoS_2 heterojunction as well as WSe_2 homojunction, utilizing CIPS as the ferroelectric control gate. These devices address the thermionic limitation encountered in conventional MOSFETs, achieving a minimum SS of 28 mV dec^{-1} for heterojunction TFETs and an impressive SS of 14.2 mV dec^{-1} for homojunction TFETs. Attributable to the high-quality and direct interaction between the ferroelectric control gate and the channel material, our homojunction device demonstrates even more exceptional capabilities. It not only manifests superior attributes in terms of basic metrics of low-power devices, such as a high switch ratio (>10^8) and a minute hysteresis window (<10 mV), but also exhibits substantial promise for diverse applications related to negative differential resistance (NDR). The demonstrated NDR phenomenon validates the underlying mechanism and features a gate-adjustable peak-to-valley current ratio (PVCR) with a remarkable value of 10.56 at room temperature (V_{CIPS} = 1.5 V), showing the prospective employment of our device within the realm of logic circuits. Additionally, the superiority of our designed concept is further confirmed through comparative experiments that make use of conventional h-BN as the dielectric gate. Our research serves as a significant demonstration of low-power devices based on ferroelectric CIPS in a fully 2D configuration.

2. Results and Discussion

By employing the novel van der Waals ferroelectric material, CIPS, as a control gate, high-quality homojunction, and heterojunction TFETs were constructed on the hafnium oxide (HfO_2) substrate. The process commenced with the mechanical exfoliation of pristine bulk crystals including WSe_2, MoS_2, and CIPS to obtain atomically thin 2D flakes. Subsequently, these materials were vertically stacked layer-by-layer utilizing the dry transfer method to create a bottom-up heterostructure.

The scanning electron microscope (SEM) images of WSe_2/MoS_2 heterojunction device and WSe_2 homojunction device are presented in **Figure 1**a,b, with CIPS stacked above a portion of the channel region to enable localized band modulation. The crystal structure of CIPS is classified under the monoclinic space group, and the vertical displacement of Cu atoms to the plane results in the generation of two different polarization states, which plays a crucial role in our devices. The vertical stacking structure and material thickness are defined using high-resolution transmission electron microscopy (TEM) in Figure S1 (Supporting Information). The thicknesses of MoS_2, WSe_2, and CIPS are measured to be 4.7, 3.6, and 64.3 nm, respectively. Figure 1c shows the Raman spectra of the mechanically exfoliated CIPS, MoS_2, and WSe_2 flakes on the SiO_2/Si substrate at room temperature. The Raman peaks of CIPS flake can be attributed to various vibration modes, including those at 106 cm^{-1} corresponding to the displacement of P–P dimers, 317 cm^{-1} due to the presence of cations. Additionally, the peaks at 264 cm^{-1} correspond to the δ(S–P–P) mode, 375 cm^{-1} to the v(p–p) mode, and 450 cm^{-1} to the v(P–S) mode. In the case of WSe_2 nanoflake, the Raman spectrum exhibits two typical peaks at 250 cm^{-1} corresponding to the E^1_{2g} mode and 261 cm^{-1} for the A_{1g} mode. The characteristic peaks for MoS_2 are observed at 383 cm^{-1} for the E^1_{2g} peak and at 405 cm^{-1} for the A_{1g} peak. We have also provided the Raman spectra for different areas of the heterojunction. The overlapping regions exhibit peaks corresponding to those of the individual materials, depending on their composition, thus confirming the effectiveness of the heterojunction. In the characterization of ferroelectric properties, the phase signal observed in the piezoresponse force microscopy (PFM) test of CIPS, as shown in Figure 1d, displays

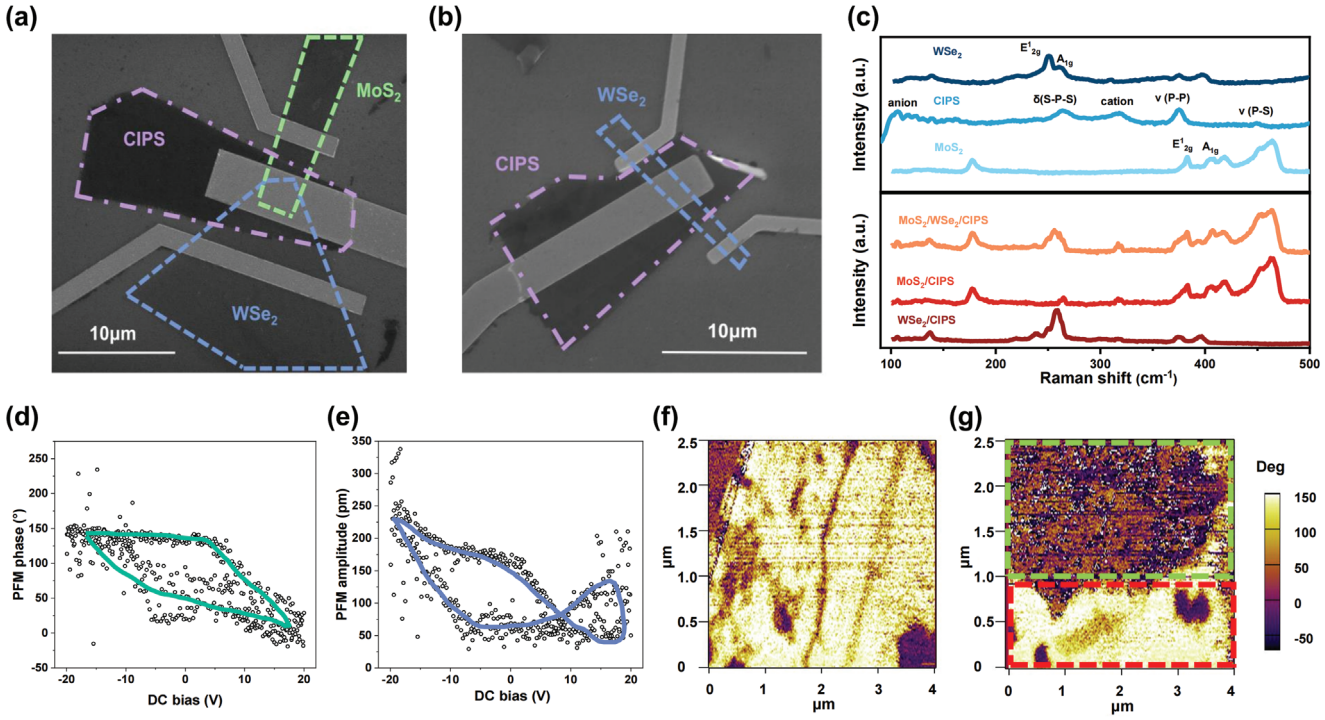

Figure 1. Characterization of heterostructures. The false-color scanning electron microscope (SEM) image of a) WSe_2/MoS_2 heterojunction device and b) WSe_2 homojunction device, each distinct color represents a specific type of material to differentiate the various components within the device. c) Raman spectroscopy (using a 633 nm laser) of the mechanically exfoliated CIPS, MoS_2 and WSe_2 flakes as well as heterojunction area on the SiO_2/Si substrate at room temperature. d) The PFM phase and e) amplitude hysteresis loops during the switching process. f) The primary PFM phase image of CIPS. g) The PFM phase image after written two-box patterns with reverse DC bias.

a clear 180° switch. Furthermore, the amplitude signal depicted in Figure 1e demonstrates a distinct butterfly loop, confirming the robust ferroelectric polarization present in the CIPS flake. To further validate the stability and controllability of ferroelectricity in our CIPS flake, we performed local polarization tests by applying bias between the conductive PFM tip and the conductive gold substrate. As shown in Figure 1f,g, opposite voltages were applied in the two designated regions marked in red and green, with the evident phase reversal serving as confirmation of polarization switching in CIPS.

The typical structure of TFETs, while similar to traditional MOSFETs, features a channel with opposite doping types near the source and drain regions. Its operational principle resembles that of a PIN diode with a gate, which controls the band bending in the channel region via the gate, thereby regulating band-to-band tunneling between the source and the channel.[30,43] Once a voltage is applied on the top control gate, the energy bands within the channel materials undergo local modulation into a staggered alignment. **Figure** 2a shows the TFET structure featuring a WSe_2/MoS_2 heterojunction as the channel, with CIPS stacked in the overlap region between WSe_2 and MoS_2. The corresponding transfer curves of the devices with the individual WSe_2 and MoS_2 as channel exhibit bipolar and n-type transfer characteristics, respectively, as shown in Figure S2 (Supporting Information). And the output characteristics of WSe_2/MoS_2 heterojunction are depicted in Figure S3b (Supporting Information). Given that MoS_2 is an n-type material, it is imperative to modulate the bipolar WSe_2 into a p-type using CIPS in order to achieve a staggered band alignment in this heterostructure. To experimentally investigate the actual impact of CIPS on heterojunction channels, electrical testing of the heterojunction TFET was conducted.

We systematically performed a series of transfer curves (V_{ds} = −1 V) under various ferroelectric gate conditions (Figure 2c), and the corresponding extracted SS is presented in Figure 2d. It is worth noting that during the scan process, the top gate applies a fixed voltage only to modulate the energy band of the channel, while the bottom gate serves as the actual scanning voltage. This distinguishes it from the previously reported NCFETs including ferroelectrics.[44,45] In our configuration, the device can fully utilize the modulating ability of the ferroelectric gate, while avoiding the introduction of noticeable hysteresis in the transfer curve. The observations reveal that, despite the steepness of the transfer curve, the corresponding SS exceeds the benchmark of 60 mV dec^{-1} upon setting V_{CIPS} to zero. In contrast, when non-zero voltages are applied to CIPS, there is a marked sharpening of the transfer curves. Simultaneously, a breakthrough of SS beyond the conventional limit of 60 mV dec^{-1} can be achieved with current variations in the range of two to three orders of magnitude, at three distinct voltages (2.5, 3, and 3.2 V). These SS data points below 60 mV dec^{-1}, are marked in the light red area represented in Figure 2d. The heterojunction TEFT demonstrates optimal performance at a V_{CIPS} of 3 V, with the minimum SS reaching a value of 28 mV dec^{-1}. These experimental results provide strong evidence for the pronounced modulation capacity of CIPS on the channel.

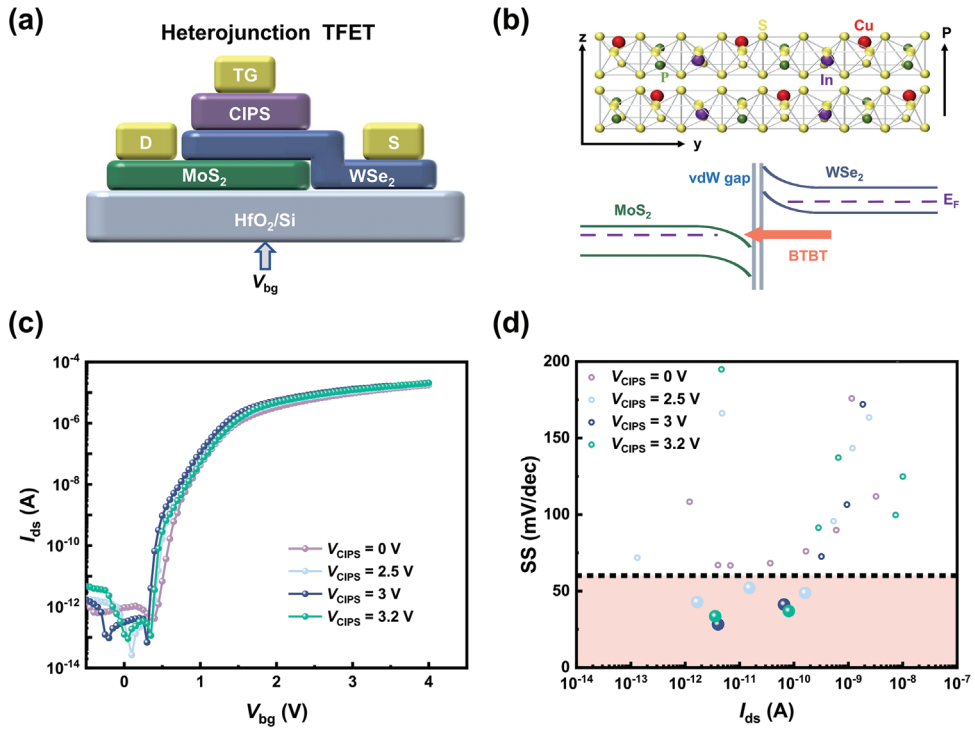

Figure 2. Schematic diagram and performance of heterojunction TFET. a) Schematic cross-section of WSe_2/MoS_2 heterojunction device. b) The upper panel shows the side view for the crystal structure of CIPS with vdW gap between the layers with the polarization direction indicated by the arrow. The lower panel shows the band alignment conditions for band-to-band tunneling. c) Transfer curves with V_{CIPS} changing from 0 V to 3.2 V at $V_{ds} = -1$ V. d) I_{ds} versus SS data extracted from the transfer curves shown in c).

The underlying mechanism was then subsequently illustrated in Figure 2b. CIPS, with an ABC-type stacked sulfur structure intercalated by elements such as copper (Cu) and indium (In) along with paired phosphorus (P-P), is used to regulate channel materials. Due to the broken symmetry in the lattice, the CIPS shows spontaneous electric polarization and ferroelectricity at temperatures below the Curie point. We maintained control over the experimental environment to ensure that the temperature remained below the Curie point of CIPS (315 K), thus safeguarding the unaltered ferroelectric properties of CIPS.[46] Characterization techniques performed at room temperature, such as PFM and Raman spectroscopy, provide additional evidence supporting the ferroelectric properties of the CIPS material utilized in our study. Applying an appropriate positive voltage on the top gate results in an upward shift of the WSe_2 band below CIPS. When the valence band of WSe_2 is positioned higher than the conduction band of MoS_2, a staggered alignment is formed between the energy bands of the two materials. Figure S4 (Supporting Information) shows the band diagram of the heterojunction at different V_{CIPS} values. Under such band alignment, the empty density of states (DOS) in the valence band of WSe_2 aligns with the occupied DOS in the conduction band of MoS_2. When a V_{ds} is applied, electrons will undergo band-to-band tunneling from the valence band of WSe_2 to the conduction band of MoS_2, resulting in the TFET being in the "on" state. It is worth noting that in the case of lightly p-doped WSe_2 with the Fermi level very close to or slightly below the valence band, there is a significant reduction in the number of electrons capable of tunneling into the n region. As a result, a smooth transition from tunneling current to thermionic emission current occurs, exhibiting only a subtle NDR trend and no breakthrough on SS. The CIPS-induced band-to-band tunneling is further substantiated through temperature-dependent measurements. As illustrated in Figure S5a,b (Supporting Information), when the temperature is varied from 290 K to 90 K, the minimum and average SS values extracted from the transfer curve exhibit a near-constant stability. Therefore, the experimental results again validate the strong modulating ability of CIPS on 2D heterojunctions.

Although the heterojunction TFET displays a lower SS that surpasses the thermal emission limit, the construction of the heterojunction inevitably introduces defects that hamper device performance. To resolve this issue, we have considered replacing the heterojunction with a homojunction. By utilizing a bipolar WSe_2 as the channel material which can be arbitrarily modulated into either p-type or n-type characteristic. Homojunction devices based on WSe_2 typically exhibit high carrier mobility, reconfigurable tunability, and ultrafast characteristics, making them suitable for low-power devices.[47,48] With the implementation of CIPS for creating a staggered band alignment, we successfully produced a homojunction TFET, as depicted in **Figure 3a**, along with the corresponding output characteristics presented in Figure S6a (Supporting Information). When the gate voltage is applied to polarize the CIPS into either an upward or downward polarized state, the WSe_2 channel beneath the controlling gate can be selectively configured into a desired doping state, thereby facilitating the formation of a homojunction. The

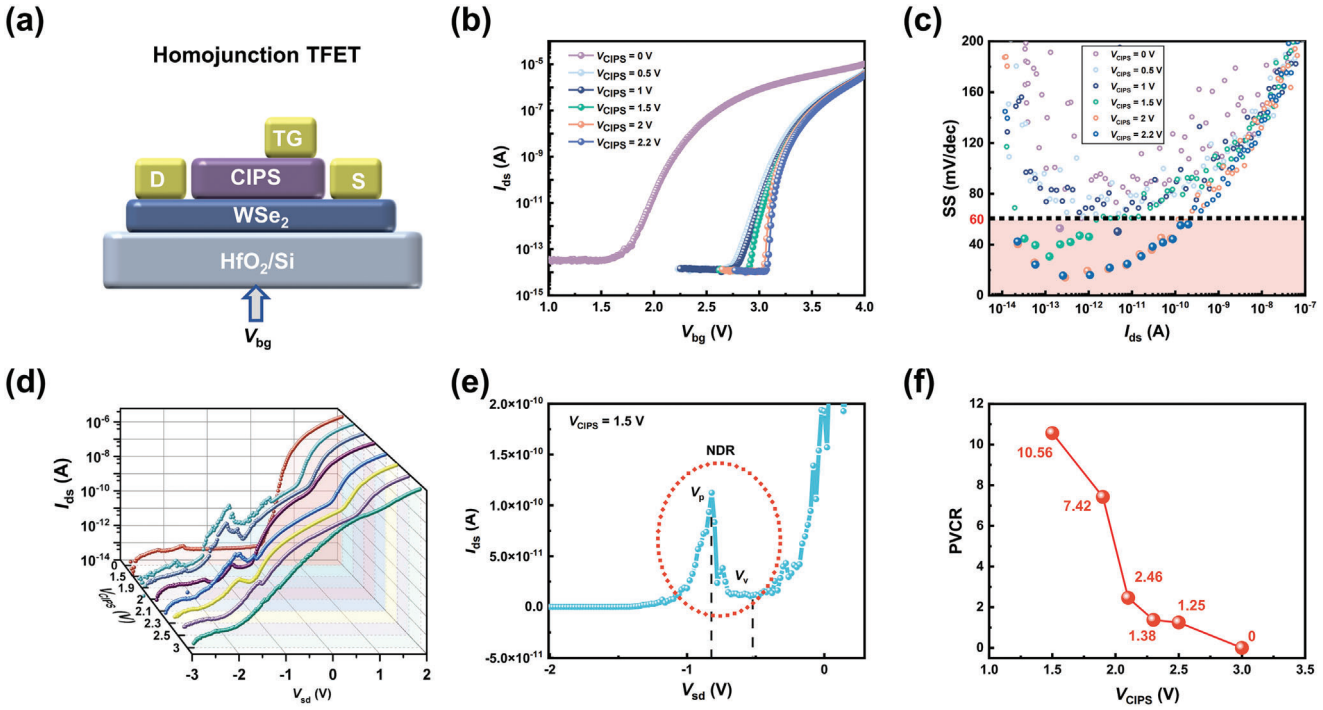

Figure 3. Schematic diagram and performance of homojunction TFET. a) Schematic cross-section of WSe_2 homojunction device. b) Transfer curves with V_{CIPS} changing from 0 V to 2.2 V at V_{ds} = 1 V. c) I_{ds} versus SS data extracted from the transfer curves shown in b). d) Output curves with V_{CIPS} changing from 0 V to 3 V. e) Output curve at V_{CIPS} = 1.5 V with significant NDR. f) V_{CIPS}-dependent PVCR extracted from the output curves shown in d).

corresponding band structure is shown in Figure S7 (Supporting Information), CIPS induces n-type or p-type doping on WSe_2 when V_{CIPS} exceeds 0 V or falls below 0 V, respectively. The mechanism of controlling n- and p-type doping in WSe_2 using ferroelectric CIPS is as described below. Downward polarization in the ferroelectric domain, induced by applying a sufficiently large positive polarizing voltage, leads to the accumulation of electrons in WSe_2, thereby achieving n-type doping as illustrated in Figure S7a (Supporting Information). Reversely, since WSe_2 is a bipolar material, p-type doping can be achieved by applying a negative polarizing voltage to the CIPS, which induces upward polarization, as depicted in Figure S7b (Supporting Information). The transfer characteristics of the obtained homojunction TFET were measured under various fixed top gate voltages. As shown in Figure 3b, a significant shift in the transfer curve is observed by applying a non-zero top gate voltage when compared to the case with zero top gate voltage, while maintaining an on/off ratio exceeding 10^8. As V_{CIPS} increases from 0 to 2.2 V, the transfer curve demonstrates a more pronounced steepness, a trend further substantiated by the corresponding SS (Figure 3c). Specifically, when the voltage applied to the top gate exceeds 1.5 V, the device can maintain an ultra-low SS of less than 60 mV dec^{-1} over a wide current range of more than three orders of magnitude. The optimal performance is achieved at V_{CIPS} = 2 V, where the minimum SS reaches 14.2 mV dec^{-1} and the average SS is approximately 30.3 mV dec^{-1}. Figure S5c,d (Supporting Information) presents the temperature-dependent measurements of the WSe_2 homojunction, the stable SS under various temperatures verify the band-to-band tunneling effect. The ultralow SS values demonstrate the effectiveness of CIPS on the construction of WSe_2 homojunction.

Upon further examination of the device's output curves at various V_{CIPS} (Figure 3d), a distinct NDR phenomenon is observed, which is the direct evidence of carrier transport dominated by band-to-band tunneling. When V_{ds} is less than V_p (the voltage at which the current reaches the peak), the filling state of the n-region conduction band and the empty state of the p-region valence band overlap, causing an increase in I_{ds}. As V_{ds} continues to increase, the overlapping states between the two regions decrease, leading to a reduction in current toward the valley point as *Vv* (the voltage at which the current reaches the valley).[19,49] Subsequently, the current exhibits a subsequent rise again as a result of the contribution of thermionic current. This phenomenon is particularly noticeable at V_{CIPS} = 1.5 V (Figure 3e). Furthermore, an analysis of the peak-to-valley current ratio (PVCR) displayed by each curve in Figure 3d was conducted, and the PVCR-V_{CIPS} plot is depicted in Figure 3f. The PVCR reaches a maximum of 10.56 when V_{CIPS} is adjusted to 1.5 V, highlighting the capacity of CIPS to effectuate a substantial doping of WSe_2. It is of paramount importance to underscore that, in contrast to the heterojunction TFET, the SS values of the homojunction TFET show a remarkable downward trend and a correspondingly pronounced NDR phenomenon. This can be principally ascribed to enhanced tunneling resulting from the superior interface cleanliness inherent to the homojunction TFET. We also investigated the modulation capability of CIPS on the MoS_2 channel (Figure S8, Supporting Information). Regrettably, while CIPS exhibited a certain level of influence on MoS_2, the impact was not as signif-

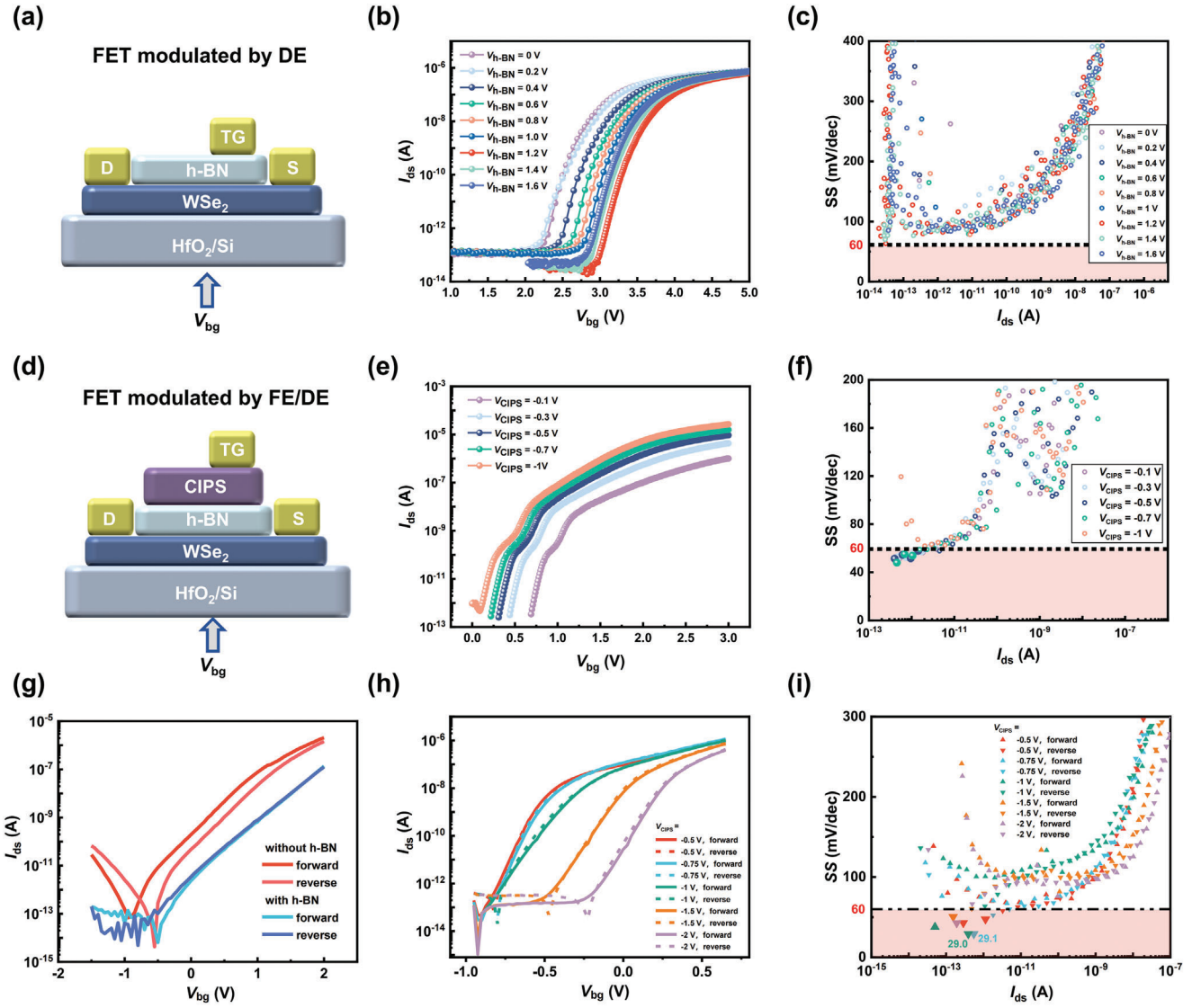

Figure 4. Schematic diagram and performance of FETs involved traditional dielectric gates. a) Schematic cross-section of WSe_2 FET modulated by h-BN. b) Transfer characteristics for various V_{CIPS} of the FET shown in (a), and c) the corresponding I_{ds} versus SS data extracted from the transfer curves. d) Schematic cross-section of WSe_2 FET modulated by both h-BN and CIPS. e) The transfer characteristics for various $V_{h\text{-}BN}$ of the FET and f) corresponding I_{ds} versus SS data extracted from the transfer curves. g) The transfer curves with and without a dielectric layer show that the introduce of h-BN significantly reduce hysteresis of 7.69 mV. h) Transfer curve of CIPS/h-BN/WSe_2 devices with negligibly small hysteresis under different V_{CIPS}. i) The SS value extracted from (h) with a minimum of 29.0 mV dec^{-1}.

icant as that for the WSe_2 homojunction. Furthermore, regardless of the different V_{CIPS} values, the SS consistently did not exceed the limit of 60 mV dec^{-1} limit. This observation aligns with our discussion that WSe_2, given its bipolar nature, can achieve band-to-band tunneling, whereas MoS_2 does not exhibit the same behavior.

Importantly, unlike previous devices showing NDR, our device exhibits a remarkably outstanding PVCR through the modulation of CIPS.[50,51] In practical applications, this suggests an improvement in the ability to distinguish thresholds within multilevel logic circuits and enhanced modulation of signal features within analog circuits. Such characteristics are essential for integrating NDR devices into operational circuits, demonstrating the enormous potential of our device for practical circuit applications.

To further validate the efficacy of our adopted framework, we also examined the scenario involving traditional dielectric gates. **Figure** 4a and Figure S9a (Supporting Information) present the schematic representation and optical image of WSe_2 FET, respectively, exclusively regulated by h-BN. By employing conventional dielectric gates to apply voltage through h-BN for localized control of WSe_2, the device not only manifests a reduced ON-state current, but also consistently achieves SS exceeding 60 mV dec^{-1} (Figure 4b,c). This confirms that the conduction mechanism of the device remains as the conventional thermionic emission and is unable to surpass the Boltzmann limit. Importantly, while the

SS did not surpass the theoretical limit, its minimum value is noticeably in close proximity to 60 mV dec^{-1}. This implies the high quality of our device fabrication and indirectly substantiates the reliability of our prior experimental results. In the device with ferroelectric/dielectric joint control (Figure 4d and Figure S9b, Supporting Information), both h-BN and CIPS are involved in the local regulation of the channel. Observations from the transfer curve (Figure 4e) and corresponding SS (Figure 4f) suggest that the control effect is notably weaker compared to the device solely controlled by CIPS, essentially failing to breach the limitation of 60 mV dec^{-1}. The presence of the h-BN dielectric layer diminishes the enhancement effect of ferroelectric gate on SS performance, as it has the potential to act as a charge isolation layer, significantly impacting the regulation effect of CIPS on the channel. The observed discrepancy in performance further confirms that the tunneling, rather than negative capacitance, is the predominant mechanism in our device.

Additionally, h-BN effectively modulates the dielectric match of the device, leading to a substantial reduction in the hysteresis of the transfer curve. By appropriately tuning the thickness of h-BN, it is possible to realize a near-hysteresis-free device, although this may come at the expense of an increase in SS (Figure 4g,h and Figure S10, Supporting Information). We have achieved a minimum SS of 29.0 mV dec^{-1} and a hysteresis window of about 7.69 mV (Figure 4h,i). In comparison to devices utilizing other channel materials, the integration of h-BN substantially mitigates hysteresis. At V_{CIPS} = 2 V, the hysteresis is observed to be negligible exclusively in the device incorporating h-BN (Figure 4h and Figures S3d, S6b, and S8d, Supporting Information). These results suggest that with further design and optimization, the device shows potential for superior performance across multiple metrics. In comparison with other low-power FETs based on ferroelectric materials recently reported, as shown in Figure S11 (Supporting Information), our homojunction TFET simultaneously demonstrates a relatively low SS, excellent on/off ratio, and an almost negligible minor hysteresis.[52–59] These findings suggest significant potential for further development and optimization in the field of semiconductor devices.

3. Conclusion

In summary, we have presented a comprehensive study on 2D TFET based on the van der Waals integration of ferroelectric CIPS with WSe_2 as well as MoS_2. Attributable to the effective modulation induced by the CIPS ferroelectric gate, both heterojunction WSe_2/MoS_2 and homojunction WSe_2 are able to achieve staggered band alignment, consequently facilitating the construction of low-power TFETs operating via band-to-band tunneling mechanism. The resulting WSe_2 homojunction TFET exhibits a minimum SS of 14.2 mV dec^{-1} and a large on/off ratio of 10^8, highlighting its potential for high-performance electronic applications. Our 2D devices effectively address the issue of defect intrusion inherent in bulk materials. By employing innovative 2D ferroelectric materials, it exhibits optimal low-power characteristics, whilst maintaining maximal simplicity in structure and manufacturing process. The device further showcases a tunable PVCR with a maximum value exceeding 10, testifying to its significant potential as an NDR device. Our findings provide strong evidence that 2D TFETs with ferroelectric gate hold significant potential as a paradigm for designing high-density and low-power devices, thereby unfolding a new trajectory towards the realization of advanced low-power apparatus.

4. Experimental Section

Device Fabrication: The MoS_2/WSe_2/h-BN/CIPS flakes were mechanically exfoliated from bulk crystals using the tape and the polydimethylsiloxane (PDMS) film. For the homojunction devices, the WSe_2 flakes were transferred on the HfO_2/Si substrate. To construct the heterojunction, the bottom layer material (MoS_2 or WSe_2) was first transferred onto the substrate. Then, utilizing the high-precision transfer platform and dry transfer method, the top layer materials were successively transferred layer by layer with the PDMS acting as a transfer supporting layer. Subsequently, electron-beam lithography technique was used to pattern the electrodes including source, drain, and gate. The Cr/Au (5/50 nm) electrodes were deposited via a thermal evaporation process at the evaporation rate of 0.2 Å s^{-1}. Finally, under the condition of 60 °C, the lift-off process took place in a hot acetone solution for a duration of 30 min.

Characterization of 2D Materials and Heterostructures: The heterostructure was characterized by scanning electron microscope. The Raman analysis of WSe_2, MoS_2, CIPS, and their heterostructures was measured using a Raman spectrometer (Horiba iHR550) with a laser wavelength of 633 nm and spot size of ≈1 µm. The PFM measurement was carried out in a commercial atomic force microscope (MFP-3D, Asylum Research, Goleta, CA) using the dual alternative voltage resonance tracking (DART) model with the drive voltage of 2 V. To confirm the vertical stacking of the heterojunction, focused ion beam (FIB) sectioning of the heterojunction was first performed, followed by energy dispersive spectroscopy (EDS) and high-resolution transmission electron microscopy (TEM) for detailed analysis.

Electrical Measurement: All electrical measurements were performed using Keithley 4200A-SCS semiconductor parameter analyzer with a probe station under vacuum at room temperature.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Keywords

2D homojunction, band-to-band tunneling, negative differential resistance, tunnel field-effect transistor, van der Waals ferroelectrics

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